Patent

Docket No.: TRAN-P004.DIV

Information Disclosure Statement Transmittal

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner of Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the below date of deposit.					
Date of Deposit:	03/29/04	Name of Person Making the Deposit:	ANTHONY CHOU	Signature of the Person Making the Deposit:	Anthony Chou

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Edmund J. Kelly, Robert F. Cmelik and Malcolm J. King

Serial No.: 09/699,947 Group Art Unit: 2186

Filed: 10/30/00 Examiner: Thai, Tuan V.

Title: TRANSLATED MEMORY PROTECTION APPARATUS FOR AN ADVANCED MICROPROCESSOR

Commissioner of Patents
P. O. Box 1450
Alexandria, VA 22313-1450
Sir:

Information Disclosure Statement Transmittal

Transmitted herewith is the following:

..... Formal drawings, totaling ..... sheets.
..... Informal drawings, totaling ..... sheets.
..... Certification for PTO Consideration
X Information Disclosure statement (2 sheets)
..... Information Disclosure statement and late filing fee
X Form 1449
..... Petition for Extension of Time
X Other: REFERENCES

Fee Calculation (for other than a small entity)

Fee Items				Fee Rate	Total
Petition for Extension of Time (fee calculated elsewhere				$ .00	$0.00
Information Disclosure Statement, late filing				$180.00	$0.00
Other:					$0.00
Total Fees					$0.00

PAYMENT OF FEES

1. The full fee due in connection with this communication is provided as follows:

[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085 .
A duplicate copy of this authorization is enclosed.

[ ] A check in the amount of $

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 29 March 2004

By: _____
Matthew J. Blecher
Reg. No. 46,558

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: TRAN-P004.DIV

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Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date
5,564,018	SYSTEM FOR AUTOMATICALLY DISTRIBUTING SELECTED MAIL ITEM TO SELECTED USER ASSOCIATED WITH OFFICE LOCATION WITHIN PHYSICAL OFFICE FLOOR PLAN IN DATA PROCESSING SYSTEM	10/08/96
5,568,614	DATA STREAMING BETWEEN PEER SUBSYSTEMS OF A COMPUTER SYSTEM	10/22/96
5,740,391	PREVENTING PREMATURE EARLY EXCEPTION SIGNALING WITH SPECIAL INSTRUCTION ENCODING	04/14/98
5,792,970	DATA SAMPLE SERIES ACCESS APPARATUS USING INTERPOLATION TO AVOID PROBLEMS DUE TO DATA SAMPLE ACCESS DELAY	08/11/98
6,079,003	REVERSE TLB FOR PROVIDING BRANCH TARGET ADDRESS IN A MICRO-PROCESSOR HAVING A PHYSICALLY-TAGGED CACHE	06/20/00
6,208,543	TRANSLATION LOOKASIDE BUFFER (TLB) INCLUDING FAST HIT SIGNAL GENERATION CIRCUITRY	03/27/01
6,266,752	REVERSE TLB FOR PROVIDING BRANCH TARGET ADDRESS IN A MICRO-PROCESSOR HAVING A PHYSICALLY-TAGGED CACHE	07/24/01
5,138,708	DIGITAL PROCESSOR USING CURRENT STATE COMPARISON FOR PROVIDING FAULT TOLERANCE	08/11/92
5,410,658	MICROPROCESSOR FOR CARRYING OUT A PLURALITY OF DIFFERENT MICROPROGRAMS AT THE SAME TIME AND METHOD FOR CONTROLLING THE MICROPROCESSOR	04/25/95
4,590,549	CONTROL SYSTEM PRIMARILY RESPONSIVE TO SIGNALS FROM DIGITAL COMPUTERS	05/20/86

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	K	EP0742512A2	11/13/96	EPO	G06F	9/38	X	
	L	WO96/30829	03/10/96	PCT	G06F	9/455	X	

The Examiner's attention is respectfully directed to the following related documents:

Ebcioglu et al.; "DAISY: DYNAMIC COMPILATION FOR 100% ARCHITECTURAL COMPATIBILITY"; IBM Thomas J. Watson Research Center Yorktown Heights, NY; 02/06/97

IBM Technical Disclosure Bulletin; "GATHERING STORE INSTRUCTIONS IN A SUPERSCALAR PROCESSOR"; XP 0006382245; Vol. 39, No. 9, Sept. 1996 pgs. 103-105

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Patent Application

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Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	5,564,018	10/08/96	Flores et al.	395	200.02	11/15/93
	B	5,568,614	10/22/96	Mendelson et al.	395	200.08	07/29/94
	C	5,740,391	04/14/98	Hunt	395	376	03/01/96
	D	5,792,970	08/11/98	Mizobata	84	607	05/30/95
	E	6,079,003	06/20/00	Witt et al.	711	200	11/20/97
	F	6,208,543	03/27/01	Tupari et al.	365	49	05/18/99
	G	6,266,752	07/24/01	Witt et al.	711	200	04/17/00
	H	5,138,708	08/11/92	Vosbury	395	575	08/03/89
	I	5,410,658	04/25/95	Sawase et al.	395	375	10/13/92
	J	4,590,549	05/20/86	Burrage et al.	364	131	05/27/83

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	K	EPO742512A2	11/13/96	EPO	G06F	9/38	X	
	L	WO96/30829	03/10/96	PCT	G06F	9/455	X	

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	M	Ebcioglu et al.; "DAISY: DYNAMIC COMPILATION FOR 100% ARCHITECTURAL COMPATIBILITY"; IBM Thomas J. Watson Research Center Yorktown Heights, NY; 02/06/97
	N	IBM Technical Disclosure Bulletin; "GATHERING STORE INSTRUCTIONS IN A SUPERSCALAR PROCESSOR"; XP 0006382245; Vol. 39, No. 9, Sept. 1996 pgs. 103-105

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.